REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1-20 are currently pending in the present application. By way of this reply, claims 1 and 8 have been amended.

II. Claim Amendments

Claims 1 and 8 have been amended to recite that each expect loop (i) is configured to expect a packet driven by the device under test within a specified time period, and (ii) picks up the expected patent if the expected packet arrives within the specified time period. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figure 5 and lines 6 – 21 on page 12 of the present application.

III. Rejection(s) Under 35 U.S.C. § 102

Claims 1-20 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,937,182 issued to Allingham (hereinafter "Allingham"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a sequence-based verification technique for verifying the functionality of hardware components that move data between nodes in a

computer system. *See* Specification, page 5, lines 16 – 18. With reference to the exemplary flow process of the present invention shown in Figure 3 of the present application, multiple drive loops drive data packets onto a device under test, where the sequence and timing of the driven data packets is determined based on timing sequence and relation criteria stored in the data packets. *See* Specification, page 9, lines 1 – 7. Further, multiple expect loops are started that are configured to expect the arrival of driven data packets from the device under test within a specified time period. *See* Specification, page 12, lines 11 – 21. If an expected data packet arrives within the specified time period, the associated expect loop picks up the expected packet. *See* Specification, page 12, lines 11 – 21. Otherwise, if the expected packet does not arrive within the specified time period, the test has failed, and an error indication is issued. *See* Specification, page 12, lines 11 – 21.

Accordingly, amended independent claims 1 and 8 of the present application require, in part, that multiple expect loops each (i) be configured to expect a data packet driven by the device under test to arrive within a specified time period, and (ii) pick up the expected packet if the expected packet arrives within the specified time period. Further, independent claim 14 of the present application requires, in part, that an expect module ensure that each expect loop satisfies specified timing and relation criteria prior to allowing the expect loop to expect and pick up a packet driven by the device under test.

Allingham, in contrast to the present invention, fails to disclose at least the limitations of the claimed invention discussed above. Applicant notes that the portions of Allingham cited by the Examiner, along with the remaining portions of Allingham, are

completely silent as to the concept or use of "expect loops." Instead, in Allingham, when an event occurs, a record of that event is transmitted to a test bench, which, in turn, compares the event record against a set of expected events stored in an expect buffer. *See* Allingham, Abstract. In Allingham, there is no disclosure or teaching of a process loop that (i) is configured to expect a data packet within a specified time period and (ii) picks up the expected packet if the expect packet arrives within the specified time period.

Further, in column 3, lines 1 – 10 of Allingham, Allingham states that one approach to check for specific orderings or timings is to configure the expect buffer to have event sequences that must occur in a specified order for them to be considered appropriate. *See also*, Allingham, column 7, lines 23 – 27. In other words, the expect buffer of Allingham may have events occurring in a particular order. However, there is no disclosure in Allingham of an "expect loop" that is configured to expect a data packet within a specified time period as required by the claimed invention. Instead, in Allingham, as an event occurs, the event is checked against a particular ordering of events in order for the event to be removed from the expect buffer. There is no process in Allingham that is configured to actively *expect* a data packet within a specified time period, where an error signal is raised if the data packet does not arrive within the specified time period.

In Allingham, if a particular event does not occur as expected, the absence of that event is not recognized until after a particular testing session has ended, thereby complicating the debugging process to determine the cause of the error. On the other hand, in the present application, expect loops are described as actively and dynamically expecting and picking up data packets as they are driven from the device under test,

where error flags are raised dependent on the success of the expect loops picking up data packets within specified time periods.

Accordingly, noting that Allingham is altogether silent, both expressly and implicitly, as to the use of "expect loops," Allingham fails to disclose a expect loop that is configured to expect a data packet driven by a device under test within a specified time period and picks up the expected packet if the expected packet arrives within the specified time period as required by the claimed invention.

In view of the above, Allingham fails to show or suggest the present invention as recited in independent claims 1 (as amended), 8 (as amended), and 14 of the present application. Thus, independent claims 1 (as amended), 8 (as amended), and 14 of the present application are patentable over Allingham. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 06145.012001;P4860).

Respectfully submitted,

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